What is claimed is:

1. An apparatus for detecting and correcting the timing skew of a data signal in a parallel data transmission system, comprising:

a data path for adjusting the timing skew of the data signal with respect to a clock signal, said data path including: a delay digital-to-analog converter (DAC), a falling edge DAC, at least two receive registers, an output multiplexer, and control logic;

a clock path for correcting the duty-cycle of a receive clock and for delaying said receive clock in normal receive operations, wherein said clock path is selectably switchable between a timing skew correction mode and a receive-data mode;

a local accurate tuning system for generating a tuning signal to tune all of the delay elements of said parallel data transmission system according to said bit-cell time;

wherein said control logic detects the timing skew of the data signal and controls said delay DAC and said falling edge DAC to provide appropriate delay to the data signal in accordance with the detected timing skew of said data signal.

2. The apparatus of claim 1, wherein said apparatus is implemented on a receive-side of said parallel data transmission system and operates substantially without control of a transmission side of said parallel data transmission system.

3. The apparatus of claim 1, wherein said local accurate tuning system comprises a local accurate clock and a delay-locked loop.

4. The apparatus of claim 1, wherein said local accurate tuning system generates a direct current (DC) tuning signal.

5. The apparatus of claim 3, wherein said delay-locked loop is locked to a frequency of said local accurate clock to produce said tuning signal.

6. The apparatus of claim 1, wherein said delay DAC delays the data signal according to said tuning signal and instructions from said control logic.

7. The apparatus of claim 6, wherein said delay DAC comprises a plurality of individual delay cells in a binary weighted arrangement such that an incremental and selectable delay is provided.

8. The apparatus of claim 1, wherein said falling edge DAC delays the falling edge of the data signal according to said tuning signal and instructions from said control logic.

9. The apparatus of claim 8, wherein said falling edge DAC comprises a plurality of individual falling-edge delay cells having at least two switchably-selected delay values, each of said plurality of falling edge cells being coupled to logic gates.

10. The apparatus of claim 1, wherein said receive registers capture data on rising and falling edges of said clock signal.

11. The apparatus of claim 1, wherein said output multiplexer swaps the outputs of said at least two receive registers according to instructions from said control logic.

12. The apparatus of claim 1, wherein said apparatus is implemented on an integrated circuit.

13. The apparatus of claim 12, wherein the integrated circuit is a digital integrated circuit.

14. An apparatus for detecting and correcting the timing skew of data in a parallel data transmission system having a receive clock and at least one data signal with a bit-cell time, the apparatus comprising:

a local accurate tuning system configured to generate a tuning signal according to the bit-cell time;

a clock path configured to correct the duty-cycle of the receive clock according to said tuning signal and said bit-cell time, wherein said clock path is selectably switchable between a timing skew correction mode and a receive-data mode;

a data path in parallel with said clock path comprising: a delay digital-to-analog converter (DAC), a falling edge DAC, at least two receive registers, an output multiplexer, and control logic;

said control logic detecting the timing skew of said at least one data signal and controlling said delay DAC and said falling edge DAC to provide appropriate delay to said data signal in accordance with the detected timing skew of said data signal with respect to said clock signal;

said delay DAC delaying said at least one data signal according to said tuning signal and instructions from said control logic;

said falling-edge DAC delaying the falling edges of said at least one data signal according to said tuning signal and instructions from said control logic;

said receive registers capturing data on both the rising and falling edges of said clock signal;

said output multiplexer swapping the outputs of said at least two receive registers according to instructions from said control logic.

15. The apparatus of claim 14, wherein said local accurate tuning system comprises a local accurate clock and a delay-locked loop.

16. The apparatus of claim 15, wherein said tuning signal is a direct current (DC) signal.

17. The apparatus of claim 15, wherein said delay-locked loop is locked to a frequency of said local accurate clock to produce said tuning signal.

18. The apparatus of claim 14, wherein said clock path comprises a de-skew path , a receive-data path, and a duty-cycle correction circuit,

the de-skew path configured to pass a clock signal from the receive clock with no delay;

the receive-data path configured to insert a delay of one-half of said bit-cell time into said clock signal;

the duty-cycle correction circuit configured to correct the duty-cycle of the receive clock to 50 percent.

19. The apparatus of claim 18, wherein said delay DAC is a variable delay circuit comprising a binary weighted arrangement of individual delay cells, each delay cell having a fixed delay period related to said bit-cell time.

20. The apparatus of claim 19, wherein the delay cells of said delay DAC provide an incremental and selectable delay.

21. The apparatus of claim 20, wherein said delay cells representing the least significant bits of said delay DAC are divided into two branches to provide said incremental and selectable delay.

22. The apparatus of claim 21, wherein the delay cells of said delay DAC are implemented as an inverter stage with transistor-implemented controlled current sources.

23. The apparatus of claim 22, wherein the current sources of said delay cells are controlled in accordance with said tuning signal.

24. The apparatus of claim 14, wherein said falling-edge DAC comprises a multi-stage variable delay circuit.

25. The apparatus of claim 14, wherein each stage of said falling-edge DAC comprises a falling-edge delay cell having at least two switchably-selected delay values coupled to logic gates.

26. The apparatus of claim 14, wherein said receive registers each comprise a D-type flip-flop.

27. The apparatus of claim 26, wherein the swapping action of said output multiplexer provides an overall de-skew time range of at least twice of said bit-cell time.

28. The apparatus of claim 14, wherein said control logic performs a binary search function, comparing the timing of said at least one stream of data with said clock signal.

29. The apparatus of claim 14, wherein the apparatus provides at least a total de-skew time range of twice of said bit-cell time with a resolution of at least six bits.

30. The apparatus of claim 14, wherein the apparatus is implemented on a digital integrated circuit.

31. A method for detecting and correcting the timing skew of data in a parallel data transmission system having a receive clock and at least one data signal with a bit-cell time, the method comprising:

generating a tuning signal having an amplitude based on a local accurate clock;

correcting the duty-cycle of the receive clock according to said tuning signal and the bit-cell time;

determining the time delay of said at least one data signal relative to the receive clock and said tuning signal;

adjusting the time delay of said at least one data signal relative to the receive clock;

adjusting the time delay of falling edges of said at least one data signal relative to said receive clock;

capturing data from said at least one data signal on the rising and falling edges of said receive clock; and

swapping the outputs of the at least two receive registers used in said capturing if the detected time-skew of said at least one data signal reaches a predetermined level.

32. The method of claim 31, wherein a delay digital-to-analog converter (DAC) used in said adjusting comprises five delay cells in a binary weighted arrangement.

33. The method of claim 32, wherein the least significant bit delay cells of said delay DAC are divided into two branches to provide an incremental and selectable delay.

34. The method of claim 33, wherein said delay cells are implemented as an inverter stage with transistor-implemented controlled current sources.

35. The method of claim 34, wherein the current sources of said delay cells are controlled in accordance with said tuning signal.

36. The method of claim 31, wherein a falling edge DAC used in said adjusting of falling edges comprises a three-stage variable delay circuit.

37. The method of claim 36, wherein each stage of said falling edge DAC comprises a falling-edge delay cell having at least two switchably-selected delay values.

38. The method of claim 31, wherein said receive registers each comprise a D-type flip-flop.

39. The method of claim 31, wherein said swapping operation provides at least a total de-skew time range of twice of said bit-cell time with a resolution of at least six bits.

40. An apparatus implemented on an integrated circuit for detecting and correcting the timing skew of at least one data signal in a parallel data transmission system, comprising:

a local accurate tuning system for generating a direct current (DC) tuning signal according to a bit-cell time of said parallel data transmission system;

a clock path for adjusting the timing and duty-cycle of a receive clock according to said DC tuning signal and said bit-cell time, wherein said clock path is selectably switchable between a timing skew correction mode and a receive-data mode;

a data path positioned in parallel with said clock path comprising: a delay digital-to-analog converter (DAC), a falling edge DAC, at least two receive registers, an output multiplexer, and control logic;

said control logic detecting the timing skew of at least one data signal and controlling said delay DAC and said falling edge DAC to provide appropriate delay to said data signal in accordance with the detected timing skew of said data signal with respect to said receive clock;

wherein said apparatus is implemented on the receive-side of said parallel data transmission system and operates substantially without control of the transmission side of said parallel data transmission system.

41. The apparatus of claim 40, wherein said delay DAC delays said at least one data signal according to said tuning signal and instructions from said control logic.

42. The apparatus of claim 40, wherein said falling edge DAC delays said at least one falling edge of at least one data signal according to said tuning signal and instructions from said control logic.

43. The apparatus of claim 40, wherein said receive registers capture data on both the rising and falling edges of said clock signal.

44. The apparatus of claim 40, wherein said output multiplexer swaps the outputs of said at least two receive registers according to instructions from said control logic.

45. The apparatus of claim 40, wherein the integrated circuit is a digital integrated circuit.